AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor integrated circuit device comprising:

a die connected to a ground lead and a power lead;

a ground plane connected to the ground lead;

an electrically insulating layer which electrically isolates said die and said ground plane;

a decoupling capacitor having a first end and a second end, the first end connected to the ground plane and the second end connected to the power lead; and

an encapsulating material which encapsulates the die and the ground plane.

2. (Previously Amended) The semiconductor integrated circuit device according to Claim 1, wherein said ground plane is adjacent a first plane of a printed circuit board for mounting electronic parts.

D1

3. (Previously Amended) The semiconductor integrated circuit device according to Claim 2, wherein said ground plane extends in two dimensions beyond the edges of said die.

4. (Previously Amended) The semiconductor integrated circuit device according to Claim 3, wherein an intra-package wiring substrate comprising wirings for a connecting path between the ground and power leads, bonding pads of the die is disposed between the die and the ground plane, and the decoupling capacitor is connected to the ground plane at one end and the power line of the intra-package wiring substrate at the other end.

5. (Original) The semiconductor integrated circuit device according to Claim 3, wherein the portion of the encapsulating material for inserting the power lead is connected to a power supply bonding pad of the die through a bonding wire at the die-side end, and the first end of the decoupling capacitor is connected to the ground plane and the second end of the decoupling capacitor is connected to the specified location of said portion for inserting

the power lead.

6. (Original) The semiconductor integrated circuit device according to Claim 5, wherein the specified location of the portion for inserting the power lead to which the decoupling capacitor is connected is the die-side end of the portion for inserting the power lead.

7. (Original) The semiconductor integrated circuit device according to Claim 5, wherein the ground plane is connected to the die-side end of the portion for inserting the power lead into the encapsulating material.

D1

8. (Original) The semiconductor integrated circuit device according to Claim 1, wherein a layer of a material having a lower dielectric constant than the dielectric constant of the encapsulating material is provided between the die and the ground plane.

9. (Original) The semiconductor integrated circuit device according to Claim 1, further comprising:

a printed circuit board for mounting electronic parts whereon the semiconductor integrated circuit device is mounted; and

an external decoupling capacitor provided on the printed circuit electrically connected in parallel with the decoupling capacitor of the semiconductor integrated circuit device.

10. (Original) An electronic apparatus or control apparatus comprising a semiconductor integrated circuit device according to Claim 1.

11. (Previously Added) The semiconductor integrated circuit device according to Claim 1, wherein the electrically insulating layer comprises one of air, encapsulating material or bonding material.

12. (Previously Added) The semiconductor integrated circuit device according to Claim 1, wherein the ground plane comprises a layer of metal.

13. (Previously Added) The semiconductor integrated circuit device according to Claim 12, wherein the layer of metal comprises copper.

14. (Previously Added) The semiconductor integrated circuit device according to Claim 1, wherein the encapsulating material encapsulates the decoupling capacitor and the electrically insulating layer.

15. (Canceled)